WHAT IS CLAIMED IS:

1: A MIS semiconductor device comprising:

a gate dielectric formed on a semiconductor substrate of a first conduction type;

a gate electrode provided on a top surface of said gate dielectric;

a first side- wall spacer formed on a surface of said semiconductor substrate spread over an outer circumference of said gate electrode, being in contact with a side wall of said gate electrode;

a first impurity area formed by introduction of first impurities having a conduction type opposite to said first conduction type into said semiconductor substrate with said gate electrode and said first side- wall spacer used as masks;

a second side- wall spacer formed by placing on a side wall of said first side- wall spacer; and

a second impurity area, which has an impurity concentration higher than an impurity concentration of said first impurity area and is formed by introduction of said first impurities into said semiconductor substrate with said gate electrode, said first side- wall spacer and said second side-wall spacer used as masks,

wherein:

said first side- wall spacer has a relative dielectric constant greater than that of said second side-wall spacer for

a predetermined width; and

one edge of said gate electrode overlaps on said first impurity area.

2: A MIS semiconductor device according to claim 1 wherein said first side- wall spacer has a predetermined width in the range from 5 nm to 15 nm.

3: A MIS semiconductor device according to claim 1 wherein said first side- wall spacer is made of a material, which can be one selected from silicon nitride, silicon, aluminum oxide, tantalum oxide, titanium oxide, zirconium dioxide and hafnium oxide.

4: A MIS semiconductor device according to claim 1 wherein a dielectric is formed between said first side- wall spacer and an upper surface of said semiconductor substrate and said gate electrode.

5: A MIS semiconductor device according to claim 1 wherein said first side- wall spacer is made of a thin film extended over an upper surface of said semiconductor substrate.

6: A MIS semiconductor device comprising:

a gate dielectric formed on a semiconductor substrate

of a first conduction type;

a gate electrode provided on a top surface of said gate dielectric;

a first side- wall spacer formed on a surface of said semiconductor substrate spread over an outer circumference of said gate electrode, being in contact with a side wall of said gate electrode;

a second side- wall spacer formed by placing on a side wall of said first side- wall spacer;

a first impurity area formed by introduction of first impurities having a conduction type opposite to said first conduction type into said semiconductor substrate with said gate electrode, said first side- wall spacer and said second side- wall spacer used as masks;

a third side- wall spacer formed by placing on a side wall of said second side- wall spacer; and

a second impurity area, which has an impurity concentration higher than that of said first impurity area and is formed by introduction of said first impurities into said semiconductor substrate with said gate electrode, said first side- wall spacer, said second side- wall spacer and said third side- wall spacer used as masks,

wherein:

said first side- wall spacer has a relative dielectric constant greater than that of said second and third side-wall

spacer for a predetermined width; and

one edge of said gate electrode overlaps on said first impurity area.

7: A MIS semiconductor device according to claim 6 wherein said first side- wall spacer has a predetermined width in the range from 5 nm to 15 nm.

8: A MIS semiconductor device according to claim 6 wherein:

said first side- wall spacer is made of a thin film extended over an upper surface of said semiconductor substrate; and

said second side- wall spacer is made of a thin film placed on a surface of said first side- wall spacer.

9: A MIS semiconductor device according to claim 1 wherein: consists of n-channel MIS semiconductor device in the p-conductive type semiconductor substrate region and p-channel MIS semiconductor device in the n-conductive type semiconductor substrate region; and at least one of n-channel MIS semiconductor device or p-channel MIS semiconductor has said first side-wall spacer.

10: A MIS- semiconductor- device- manufacturing method comprising:

a process of forming a gate dielectric on a semiconductor

substrate of a first conduction type;

a process of providing a gate electrode on a top surface of said gate dielectric;

a process of forming a first side- wall spacer on a surface of said semiconductor substrate spread over an outer circumference of said gate electrode, being in contact with a side wall of said gate electrode by placing a dielectric for a predetermined width;

a process of formation of a first impurity area by introduction of first impurities having a conduction type opposite to said first conduction type into said semiconductor substrate with said gate electrode and said first side- wall spacer used as masks;

a process of formation of a second side- wall spacer by placing on said first side- wall spacer;

a process of forming a second impurity area having an impurity concentration higher than an impurity concentration of said first impurity area by introduction of said first impurities into said semiconductor substrate with said gate electrode, said first side- wall spacer and said second side-wall spacer as masks whereby said first side- wall spacer is made of a material having a relative dielectric constant greater than that of said second side- wall spacer; and

a process of carrying out a heat treatment on said first impurity area to overlap one edge of said gate electrode on

said first side-wall spacer.

11: A MIS- semiconductor- device- manufacturing according to claim 10 whereby said first side-wall spacer is made of a material, which can be one selected from silicon nitride, silicon, aluminum oxide, tantalum oxide, titanium oxide, zirconium dioxide and hafnium oxide.

12: A MIS- semiconductor- device- manufacturing according to claim 10 whereby said first side- wall spacer is made of a thin film having a fixed thickness.